Guest Lecture/Training on
"VLSI Physical Design, SoCs, RTL Design, and Synthesis"
by Mr. Abhishek Nigam, Mr. Sohang, Mr. Ankit Mittal, and Mr. Rishabh

Introduction

The event on "VLSI Physical Design, System on Chips (SoCs), Register Transfer Level (RTL) Design, and Synthesis" was conducted to provide participants with an in-depth understanding of key concepts in VLSI design and semiconductor technology. The event brought together industry experts, researchers, and students to discuss advancements, methodologies, and practical applications in the field. The primary objective was to bridge the gap between theoretical knowledge and practical implementation in chip design.

Event Details

Date and Venue: The event took place on 16 March 2025 at FAB-LAB, SOE, DEI.
Organizers: The session was organized by Mr. Abhishek Nigam (HCL Tech), with contributions from academic and industry professionals specializing in VLSI design and semiconductor technology.
Audience: The event was attended by students, faculty members, and professionals from various engineering backgrounds, including electronics, computer science, and embedded systems.

Key Sessions and Discussions

Lecture by Mr. Abhishek Nigam (HCL Tech)

The event featured an expert panel discussion, where industry leaders from semiconductor companies shared insights into the latest trends in VLSI design. Topics such as AI-driven chip design, low-power SoCs, and the impact of Moore's Law on future semiconductor development were addressed. Experts also provided career guidance, emphasizing the skills required for a successful career in VLSI and chip design.

Topic : System on Chips (SoCs)

This session explored the architecture and design of SoCs, emphasizing their significance in modern computing and embedded systems. Speakers discussed the integration of multiple components, including processors, memory units, and peripherals, into a single chip. Case studies on SoC implementations in smartphones, IoT devices, and automotive applications were presented, demonstrating real-world applications and design challenges.

Lecture by Mr. Ankit Mittal (Qualcomm)

Topic : Register Transfer Level (RTL) Design &Synthesis

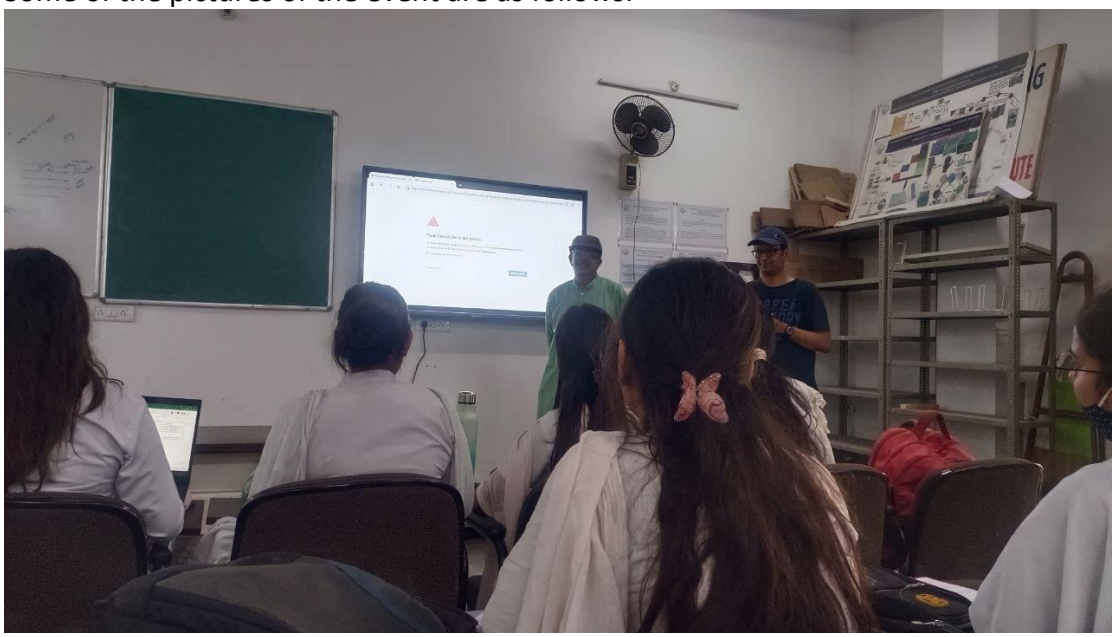
RTL design was explained in detail, focusing on the process of translating high-level algorithms into hardware descriptions using Hardware Description Languages (HDLs) like Verilog and VHDL. The session included hands-on demonstrations where participants analyzed RTL code, simulated designs, and optimized hardware performance. The importance of power-aware RTL coding and design verification techniques was also highlighted.

The session on Synthesis covered the process of converting RTL code into gate-level representations. Participants gained insights into logic synthesis techniques, technology mapping, and timing constraints. Discussions on static timing analysis (STA) and power analysis were particularly engaging, as experts provided practical guidelines on achieving design efficiency and meeting fabrication constraints.

Lecture by Mr. Rishabh Banerjee (ARM)
Topic : Physical Design
The session on Physical Design covered essential topics such as floor planning, placement, routing, clock tree synthesis (CTS), and power optimization. Experts highlighted the challenges in modern physical design, particularly in advanced technology nodes like 7nm and below. The discussion also included the impact of process variations and how Electronic Design Automation (EDA) tools play a crucial role in optimizing layouts.

<u>Conclusion and Feedback</u>
The event concluded with a summary of key takeaways and an open Q&A session, allowing participants to clarify doubts and seek further insights. Feedback from attendees was overwhelmingly positive, with many appreciating the practical exposure and industry relevance of the topics covered. Suggestions for future events included more advanced hands-on training sessions and guest lectures from semiconductor industry pioneers.
Overall, the event successfully provided a comprehensive understanding of Physical Design, SoCs, RTL, and Synthesis, equipping participants with valuable knowledge and skills applicable in the semiconductor industry.

Some of the pictures of the event are as follows:



1. Address by the Director Sir to the Students on the Event with Guest Mr. Abhishek Nigam.

2. Lecture by Mr. Sohang.

3. Lecture by Mr. Ankit Mittal.

4. Lecture by Mr. Rishabh.

5. Group Photo of Student Attendees.

6. Group Photo of the Students with Guest Speakers.