INVITATION FOR QUOTATION

TEQIP-III/2018/deia/Shopping/5 **03-Jul-2018**

Sub: Invitation for Quotations for supply of Goods

Dear Sir,

1. You are invited to submit your most competitive quotation for the following goods with item wise detailed specifications given at Annexure I,

Sr. No	**Brief Description**	**Quantity**	**Delivery Period(In days)**	**Place of Delivery**	**Installation Requirement (if any)**
1	Mentor Design Tools, server and storage solutions	1	30	DEI, Agra	Complete setup

2. Government of India has received a credit from the International Development Association (IDA) towards the cost of the **Technical Education Quality Improvement Programme[TEQIP]-Phase III** Project and intends to apply part of the proceeds of this credit to eligible payments under the contract for which this invitation for quotations is issued.
3. Quotation,

   3.1 The contract shall be for the full quantity as described above.

   3.2 Corrections, if any, shall be made by crossing out, initialing, dating and re writing.

   3.3 All duties and other levies payable by the supplier under the contract shall be included in the unit price.

   3.4 Applicable taxes shall be quoted separately for all items.

3.5 The prices quoted by the bidder shall be fixed for the duration of the contract and shall not be subject to adjustment on any account.

3.6 The Prices should be quoted in Indian Rupees only.

4. Each bidder shall submit only one quotation.
5. Quotation shall remain valid for a period not less than **55** days after the last date of quotation submission.
6. Evaluation of Quotations,

   The Purchaser will evaluate and compare the quotations determined to be substantially responsive i.e. which

   6.1 are properly signed ; and

   6.2 confirm to the terms and conditions, and specifications.
7. The Quotations would be evaluated for all items together.
8. Award of contract:

   The Purchaser will award the contract to the bidder whose quotation has been determined to be substantially responsive and who has offered the lowest evaluated quotation price.

   8.1 Notwithstanding the above, the Purchaser reserves the right to accept or reject any quotations and to cancel the bidding process and reject all quotations at any time prior to the award of contract.

   8.2 The bidder whose bid is accepted will be notified of the award of contract by the Purchaser prior to expiration of the quotation validity period. The terms of the accepted offer shall be incorporated in the purchase order.
9. Payment shall be made in Indian Rupees as follows:

   Delivery and Installation - 90% of total cost

   Satisfactory Acceptance - 10% of total cost

10. All supplied items are under warranty of **60** months from the date of successful acceptance of items.
11. You are requested to provide your offer latest by **10:00** hours on **16-Jul-2018 .**

12. Detailed specifications of the items are at Annexure I.
13. Training Clause (if any) **Traingin is required**
14. Testing/Installation Clause (if any) **Product installation, configuration, support for getting PDK from foundry, pdk configuration, phone/email product support**
15. Information brochures/ Product catalogue, if any must be accompanied with the quotation clearly indicating the model quoted for.
16. Sealed quotation to be submitted/ delivered at the address mentioned below,
    Dayalbagh, Agra - 282005, Uttar Pradesh
17. We look forward to receiving your quotation and thank you for your interest in this project.

Amol Gupta
9897860992 , amolgupta87@gmail.com
(Authorized Signatory)
Name & Designation

Annexure I

Sr. No	Item Name	Specifications
1	Mentor Design Tools, server and storage solutions	EDA Tools chain with PCB Design Software complete solution 1) Back End IC flow SDL tool , IC assembles for floor planning A-route for automatic routing Provides necessary tie between physical verification streamlined design flow for AMS SoC design Efficient handoff between IC design and manufacturing. Supports hierarchical logic design Built-in extractor which generates a SPICE netlist from the schematic diagram XRC for parasitic extraction LVS for layout vs. schematic. Facility for generation of user defined symbols for schematic entry MOS level schematic support. Sub-micron, deep-submicron, nano scale technology support Generation of the schematic for layout generation & editing from verilog gate level Net list. Single, streamlined design flow for AMS SoC design Design-error-free cell library. Can quickly output designs in SPICE, HSPICE, or Verilog netlist formats Operates on Linux OS with full UNIX data compatibility Full-chip RF IC verification for wireless applications. Analog Mixed

		Signal Simulation and Analysis. Reuse of unmodified legacy code is facilitated Allows designers to create IC layouts based on information from a logic source Makes navigation between the layout and schematic fast and easy Built-in SPICE-like analog simulator features fast time-domain, voltage and current estimation, with very intuitive post processing: frequency estimation, delay estimation. Gives layout engineers full control of circuit density and performance, while improving productivity Offers AMS SoC designers a single parasitic extraction solution that is independent of design style or flow It must have Antenna design tools also. Provides manageable netlists and mixed-level outputs for ease of re-simulation without loss of accuracy Real-case measurement data-base in 0.7,0.35, 0.25 and 0.18µm for comparison with models Convenient Monte-carlo simulation Unparalleled performance and capacity Supports BSIM3, BSIM4 MOS models Change the model parameters and see their effects on Id/Vd, Id/Vg Id(log)/Vg, threshold vs Length 2) Front End Tools High-performance solution built on the best-in-class HDL simulator which supports VHDL, SystemVerilog, Verilog, SystemC, and PSL Supports SystemVerilog and PSL assertions for improving quality Supports SystemVerilog constrained-random functionality for improving productivity Language neutrality supports any combination of VHDL, Verilog, SystemVerilog and EDIF usage Synthsis tool, one easy learning curve, one set of scripts for CPLDs, FPGAs (Xilinx, Cypress FPGA IC Support), or ASICs Provides high quality of results with the speed and features needed for large designs True hierarchical support makes it easy to group and ungroup design elements, which can then be targeted for single or multiple chips Offers users language neutrality, and both platform- and target device independence Leonardo Insight schematic viewer accelerates synthesis analysis Works with the DFT tool suite to ensure automated, whole chip test Flexible and powerful test synthesis and analysis for any design flow Test Kompress, ATPG, SCAN Chain ion tool for DFT. 3) PCB Design & Analysis Tools Should contain online portal to download Symbols, IPC compliant footprints of the latest components directly into the Library. The portal should contain at least 850k components Should be able to be import MRP/ERP databases through industry-standard ODBC (Open Database Connectivity). Should be able to import MRP/ERP databases in various formats such as text, spreadsheets, Microsoft Access, Oracle, SQL

		Server Should analyze the design and verify the components with respect to Assembly quantity and provide natives in case of insufficiency Should be searchable for different search criteria and should offer suitable components/part natives. Should be able to facilitate legacy Netlist methodology and latest Integrated methodology for PCB design under the same license Should allow defining at least 50 design rules and perform design rule check (DRC) in schematic level. Should contain easy Schematic alignment options and perform rule check for graphics, texts, alignment, etc. Should allow Logical definition and management of variants in the Schematic and also able to create variant outputs like BOM, Netlist, etc for the Variant schematics Should contain in-built videos conveying the functionality of the tools. Should facilitate standard DC, Transientand Frequency response analysis Should facilitate generation of simulation report in.txt or .csv format and saving response waveform as image file (JPG/BMP) Signal Integrity Analysis Module Layout &Router Tool Project Database management Thermal Analysis Module All License must be for 100 Users Floating License for 03/05/more Years Based on budget exact order will be decided

FORMAT FOR QUOTATION SUBMISSION

(In letterhead of the supplier with seal)

Date: _____

To:

_____

_____

Sl. No.	Description of goods (with full Specifications)	Qty.	Unit	Quoted Unit rate in Rs. (Including Ex Factory price, excise duty, packing and forwarding, transportation, insurance, other local costs incidental to delivery and warranty/ guaranty commitments)	Total Price (A)	Sales tax and other taxes payable	
						In %	In figures (B)
Total Cost							

Gross Total Cost (A+B): Rs. _____

We agree to supply the above goods in accordance with the technical specifications for a total contract price of Rs. ———————— (Amount in figures) (Rupees ————————amount in words) within the period specified in the Invitation for Quotations.

We confirm that the normal commercial warranty/ guarantee of ——————— months shall apply to the offered items and we also confirm to agree with terms and conditions as mentioned in the Invitation Letter.

We hereby certify that we have taken steps to ensure that no person acting for us or on our behalf will engage in bribery.

Signature of Supplier

Name: _____

Address: _____

Contact No: _____